

L Number	Hits	Search Text	DB	Time stamp
1	52	(wafer with dicing) and ((chips or wafer) with interposer)	USPAT; US-PGPUB	2002/06/04 09:28
2	44	((wafer with dicing) and ((chips or wafer) with interposer)) and test\$3	USPAT; US-PGPUB	2002/06/04 09:28

DOCUMENT-IDENTIFIER: US 6136681 A
TITLE: Tool used in forming a chip scale package

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ABPL:

A method of assembling a plurality of semiconductor chips is provided. A portion of a semiconductor wafer containing the plurality of chips is provided. Each of the plurality of chips has a contact pattern area including a pattern of contacts on a surface of the chip. A respective section of a dielectric interposer is assembled to each respective one of the plurality of chips individually, without detaching the plurality of chips from the portion of the semiconductor wafer. Each section of interposer has a plurality of bonding pads near an outer periphery of the section, so that each bonding pad lies near the contact pattern area of the corresponding one of the plurality of chips. Each bonding pad is wire bonded to a respective one of the contacts on the front surface of the corresponding one of the plurality of chips. The bonding step includes: (1) bonding one end of each wire to a respective bonding pad of the interposer using micro-resistant welding or ultrasonic bonding, and (2) bonding the other end of each wire to a respective contact of the chip using ultrasonic bonding. If a defective bond is detected, a wire may be removed and replaced by wire bonding. An encapsulant is applied to encapsulate the wires on each of the plurality of chips. The encapsulated chips are cut from the semiconductor wafer. Wires may be bonded at the corners of the chip, and need not be perpendicular to the sides of the chip.

BSPR:

The '861 Patent generally describes a wafer level integration process, in which, instead of attaching a multiplicity of cut chips to a long tape, individual interposers, similar to the interposer described above with reference to the '861 Patent, are positioned on each chip, individually, while the chips are still on the wafer. The interposers are assembled to the chips before the chips are separated from the wafer. The contacts on each chip are secured to the terminals of each interposer and the contacts of each chip are encapsulated. The individual chips are separated from the wafer and from one another by cutting the wafer using a conventional wafer severing or "dicing" equipment. This process yields a plurality of chip and interposer subassemblies.

BSPR:

Wafer level integration is desirable, because the wafer is a rigid body, allowing more accurate and predictable registration for all fabrication processes prior to the dicing step. However, improved wafer level integration techniques are desired.

BSPR:

The present invention is a method of assembling a plurality of semiconductor chips. A portion of a semiconductor wafer containing the plurality of chips is provided. Each of the plurality of chips has a contact pattern area including a pattern of contacts on a surface of the chip. A respective section of a flexible sheetlike dielectric interposer is assembled to each respective one of the plurality of chips individually, without detaching the plurality of chips from the semiconductor wafer. Each section of interposer has a plurality of

bonding pads near an outer periphery of the section, so that each bonding pad lies near the contact pattern area of the corresponding one of the plurality of chips. Each bonding pad is wire bonded to a respective one of the contacts on the front surface of the corresponding one of the plurality of chips. An encapsulant is applied to encapsulate the wires on each of the plurality of chips. The encapsulated chips are cut from the semiconductor wafer.

DRPR:

FIG. 2B shows the wafer portion of FIG. 2A after an interposer and a compliant material applied to each die.

DRPR:

FIG. 2C shows the wafer portion of FIG. 2B after wire bonding the pads of each interposer to the contacts of the corresponding chip.

DRPR:

FIG. 2E shows the wafer portion of FIG. 2D after applying a solder ball to each respective land on the top surface of the interposer.

DEPR:

Prior to the integration of the devices 101, each chip on wafer 100 is tested using conventional electrical test equipment, and any defective chips are identified. The tests determine whether each individual chip 100a, 100b etc. on the portion of the semiconductor wafer 100 complies with a predetermined set of acceptance criteria. Preferably, only those chips which comply with the electrical acceptance criteria are included in the plurality of chips that are processed in the manner shown in FIGS. 2A-2G. Any chips that are determined to be defective may be marked prior to the package fabrication process, and remain unpackaged on the wafer until the completion of the fabrication and cutting

steps shown in FIGS. 2A-2F. Following the cutting (dicing) step of FIG. 2F, the defective chips may be discarded.

DEPR:

A section 106 of a dielectric interposer is assembled on each respective one of the plurality of chips 100a, 100b, individually, without detaching the plurality of chips 100a, 100b from the semiconductor wafer 100. As shown in FIGS. 2B-2G, the interposer 106 may be formed from two sheets of a flexible material. Each section 106 of the interposer has a plurality of bonding pads 103 near an outer periphery of the section. The thickness of pads 103 has been exaggerated for easy visibility in FIGS. 2B-2F, but one of ordinary skill in the art of semiconductor packaging understands that the pads 103 and the leads 107 connected to pads 103 are formed of a thin film on the interposer 106 using a conventional additive or subtractive technique, such as plating or etching, in the same manner as the leads 107 and the solder ball lands 107. As best seen in FIG. 3, each bonding pad 103 lies near a respective contact 102 in the contact pattern area of the corresponding of chip 100a. Thus, it is possible to construct a chip scale package 101 that is only slightly larger in area than the area of a bare die or flip chip (not shown) would be.

DEPR:

FIG. 2E shows wafer portion 100 after application of solder balls 112 to the top surface of interposer 106. Typically, a conventional solder flux is used to prepare the ball lands 107 on the surface of the interposer section 106, so that the solder bonds properly to the ball lands 107 of interposer 106. The solder balls may be approximately 280 micrometers high.

DEPR:

The inventor has determined that one of the difficulties of fabricating micro BGA type CSPs in a tape automated bonding process (with a plurality of individual chips bonded onto a linear tape such as that described in the U.S. Pat. No. 5,346,861 referenced above) is the difficulty in aligning the chip properly on the tape. The tape (interposer) in the '861 Patent has the locations of all of the bonding pads on the surface of the interposer fixed with respect to one another. The alignment of the chip on the interposer controls whether each one of the electrical connections between the terminals of the interposer and the contacts of the chip can be made successfully without great difficulty. To ensure that the terminals of the interposer are aligned properly with the contacts of the chip. each chip must be glued on with an accuracy of under 10 micrometers. Similarly, in the embodiment described in the '861 Patent in which individual interposer sections are bonded onto an uncut semiconductor wafer, it is still necessary to attach the interposer sections with less than 10 micrometer accuracy to ensure that all of the terminals in the interposer sections are properly aligned with the respective chip contacts to which they must be bonded.

DEPR:

By using fine wire interconnections 108, the invention achieves several advantages. One advantage is that the placement accuracy of the interposer on the wafer can be relaxed from about ± 10 micrometers to about ± 50 micrometers. Any increased error in alignment can be corrected by the wire bonding process, because the position at which each wire is connected can be adjusted. Because the placement accuracy requirements for wire bonding are

substantially less stringent, it is possible to increase the production speed relative to prior art systems without sacrificing yield. The inventor believes that an increase in production from approximately 750 units per hour for a Micro BGA type process to approximately 5000 units per hour using the Wafer-level Micro BGA process according to the invention. This advantage of the invention may be contrasted to the fixed position of the printed wirings that were integrally formed on the interposer in the '861 Patent.